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WE CLAIM:

- 1 1. A method for cooling an electronic system, comprising:  
2 detecting a plurality of digital events indicative of electronic system operations and  
3 heat generated during the operations;  
4 accumulating a count of a subset of the plurality of digital events in a counting  
5 circuit, the subset of digital events occurring within a sampling window time interval; and  
6 controlling a cooling arrangement responsive to the counting circuit, wherein the  
7 cooling arrangement is adapted to cool the electronic system.
- 1 2. The method of claim 1, wherein the counting circuit is a binary counter.
- 1 3. The method of claim 1, wherein the counting circuit is a capacitor and further  
2 comprising adding a substantially fixed amount of charge to the capacitor responsive to  
3 each digital event in the subset.
- 1 4. The method of claim 3, further comprising switching a transistor on to conduct  
2 current from a constant current source to the capacitor responsive to each digital event in  
3 the subset.
- 1 5. The method of claim 4, wherein the transistor is biased to operate in a constant  
2 current region by the capacitor.
- 1 6. The method of claim 5, wherein the sampling window time interval has a fixed  
2 duration and is within a base time interval, the base time interval being a periodic time  
3 interval having a fixed duration and period.
- 1 7. The method of claim 6, further comprising selecting the sampling window time  
2 interval at a pseudo-random time within the base time interval.
- 1 8. The method of claim 1, wherein the counting circuit has a threshold and further  
2 comprising providing a counting circuit output signal responsive to the count of digital

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3 events in the subset accumulated and the threshold, the cooling arrangement responsive to  
4 the output signal.

1 9. The method of claim 8, wherein the threshold is variable.

1 10. The method of claim 9, wherein the threshold is selectable.

1 11. The method of claim 10, wherein the threshold is programmable.

1 12. The method of claim 1, further comprising regulating the cooling arrangement to  
2 provide more electronic system cooling in proportion to the count of digital events in the  
3 subset accumulated in the counting circuit.

1 13. The method of claim 1, further comprising monitoring an electronic system bus  
2 logic signal wherein a digital event is a logic signal transition.

1 14. The method of claim 13, wherein the electronic system bus is a data bus.

1 15. The method of claim 13, wherein the electronic system bus is an address bus

1 16. A method for monitoring an electronic system and controlling an operating  
2 parameter, comprising:  
3 detecting a plurality of digital events indicative of electronic system operations;  
4 selecting a subset of the plurality of digital events, the subset of digital events  
5 occurring within a sampling window time interval;  
6 switching a transistor on responsive to each digital event of the subset to conduct  
7 current from a constant current source to a capacitor, the transistor being biased to operate  
8 in a constant current region;  
9 adding a substantially fixed amount of charge to the capacitor responsive to each  
10 digital event of the subset;  
11 accumulating a charge in the capacitor representative of a count of digital events in  
12 the subset; and

13 controlling the operating parameter responsive to the charge accumulated in the  
14 capacitor.

1 17. The method of claim 16, further comprising biasing the transistor with the capacitor  
2 to operate in a constant current region.

1 18. The method of claim 17, wherein the sampling window time interval has a fixed  
2 duration within a base time interval and the base time interval is a periodic time interval  
3 having a fixed duration and period.

1 19. The method of claim 18, further comprising selecting the sampling window time  
2 interval at a pseudo-random time within the base time interval.

1 20. An electronic system, comprising:  
2 means for detecting a plurality of digital events indicative of electronic system  
3 operations and heat generated during the operations;  
4 means for accumulating a count of a subset of the plurality of digital events in a  
5 counting circuit, the subset of digital events occurring within a sampling window time  
6 interval; and  
7 means for controlling a cooling arrangement responsive to the counting circuit,  
8 wherein the cooling arrangement is adapted to cool the electronic system.

1 21. An electronic system having an controllable operating parameter, comprising:  
2 means for detecting a plurality of digital events indicative of electronic system  
3 operations;  
4 means for selecting a subset of the plurality of digital events, the subset of digital  
5 events occurring within a sampling window time interval;  
6 means for switching a transistor on responsive to each digital event of the subset to  
7 conduct current from a constant current source to a capacitor, the transistor being biased to  
8 operate in a constant current region;  
9 means for adding a substantially fixed amount of charge to the capacitor responsive  
10 to each digital event of the subset;

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11 means for accumulating a charge in the capacitor representative of a count of digital  
12 events in the subset; and

13 means for controlling the operating parameter responsive to the charge accumulated  
14 in the capacitor.

1 22. The electronic system of claim 21, further comprising means for selecting the  
2 initiation of the sampling window time interval at a pseudo-randomly time within a base  
3 time interval, wherein the sampling window time interval has a fixed duration and the base  
4 time interval is a periodic time interval having a fixed duration and period.

1 23. An electronic system, comprising:  
2 a cooling arrangement;  
3 a signal path disposed within the electronic system, the signal path conducting a  
4 logic signal;  
5 a detection circuit communicatively coupled to the signal path and arranged to  
6 detect digital events derived from the logic signal,  
7 a sampling circuit coupled to the detection circuit and arranged to select a subset of  
8 the digital events, and  
9 a counting circuit coupled to the sampling circuit and adapted to accumulate a count  
10 of digital events in the subset; and  
11 a control circuit coupled to the cooling arrangement and the counting circuit, the  
12 control circuit adapted to regulate the cooling arrangement responsive to the count of  
13 digital events in the subset accumulated.

1 24. The electronic system of claim 23, wherein the counting circuit is a binary counter.

1 25. The electronic system of claim 23, wherein the counting circuit is a constant current  
2 source coupled through a switched transistor to a capacitor.

1 26. The electronic system of claim 25, wherein the sampling circuit is arranged to  
2 pseudo-randomly select the subset of the digital events during a periodic base time interval  
3 having a fixed duration.

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1 27. The electronic system of claim 23, further comprising a memory arrangement and a  
2 memory controller, wherein the signal path is a bus communicatively coupling the memory  
3 arrangement to a memory controller.

1 28. The electronic system of claim 27, wherein the counting circuit is a constant current  
2 source coupled through a switched transistor to a capacitor.

1 29. The electronic system of claim 28, wherein the sampling circuit is arranged to  
2 pseudo-randomly select a subset of the digital events during a periodic base time interval  
3 having a fixed duration.

1 30. The electronic system of claim 29, further comprising a central processing unit  
2 ("CPU") communicatively coupled to the memory controller.

1 31. The electronic system of claim 30, further comprising a driver circuit coupled to the  
2 control circuit, wherein the control circuit is adapted to communicate control signals to the  
3 driver circuit responsive to the counting circuit, and the driver circuit is adapted to control  
4 the cooling arrangement responsive to the control signals.